Docket No.: 740819-640

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	)	
Tsuneo IKURA	)	Group Art Unit: 2822
Application No. 09/942,907	)	Examiner: Toniae M. Thomas
Filed: August 31, 2001	)	Confirmation No. 8137
For: METHOD FOR FABRICATING SEMICONDUCTOR DEVICE	)	Date: February 20, 2004

TRANSMITTAL OF VERIFIED ENGLISH TRANSLATION OF PRIORITY DOCUMENT

Assistant Commissioner for Patents
Alexandria, VA 22313

Sir:

Filed concurrently with the Request for Reconsideration submitted on February 20, 2004, submitted herewith is an English Translation of Japanese Priority Document No. 2000-362300 with Declaration. Consideration is respectfully requested.

Acknowledgment is respectfully requested.

Respectfully submitted,

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DECLARATION

I, the undersigned, of 6-1-201, Futamicho, Nishinomiya-shi, Hyogo, Japan, hereby certify that I am well acquainted with the English and Japanese languages, that I am an experienced translator for patent matter, and that the attached document is a true English translation of

Japanese Patent Application No. **2000-362300**

that was filed in Japanese.

I declare that all statements made herein of my own knowledge are true, that all statements on information and belief are believed to be true, and that these statements were made with the knowledge that willful statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Signature:

Masahiro Yamasaki

Masahiro Yamasaki

Dated: **January 23, 2004**

[Name of the Document] Specification

[Title of the Invention] Method for fabricating semiconductor device

[Claims]

[Claim 1] A method for fabricating a semiconductor device, the method characterized by comprising the steps of:

forming, on a substrate, a first insulating film with a relatively low dielectric constant and low mechanical strength;

forming a mask pattern on a region of the first insulating film where capacitance between interconnects is desired to be lowered, and then patterning the first insulating film by performing selective etching using the mask pattern;

forming, over the substrate, a second insulating film with a relatively high dielectric constant and high mechanical strength;

planarizing the second insulating film by polishing so that the second insulating film thinly remains on the surface of the first insulating film;

forming an interconnect groove in the first insulating film; and

forming a buried interconnect in the interconnect groove.

[Claim 2] The semiconductor device fabricating method of Claim 1, characterized by further comprising the step of forming, over the first insulating film in which the buried interconnect is formed, a third insulating film for preventing diffusion of a metal included in the buried interconnect.

[Claim 3] The semiconductor device fabricating method of Claim 1, characterized in that:

the first insulating film and the second insulating film each include an inorganic material as a principal constituent; and

the step of forming the interconnect groove in the first insulating film comprises the step of forming an interconnect groove also in the second insulating film by selectively etching the first insulating film and the second insulating film at the same time.

[Claim 4] The semiconductor device fabricating method of Claim 1, characterized in that:

the first insulating film includes an organic material as a principal constituent while the second insulating film includes an inorganic material as a principal constituent; and

the method further comprises, before or after the step of forming the interconnect groove in the first insulating film, the step of forming an interconnect groove in the second insulating film by selectively etching the second insulating film.

[Claim 5] The semiconductor device fabricating method of Claim 1, characterized in that a portion of the second insulating film, which thinly remains on the surface of the first insulating film, has a thickness of 10 nm to 50 nm.

[Claim 6] A method for fabricating a semiconductor device, the method characterized by comprising the steps of:

forming, on a substrate, a first insulating film with a relatively low dielectric constant and low mechanical strength;

forming, on the first insulating film, a second insulating film having mechanical strength higher than that of the first insulating film;

forming a mask pattern on a region of the second insulating film where capacitance between interconnects is desired to be lowered, and then patterning the second insulating film and the first insulating film by selectively etching the second insulating film and the first insulating film using the mask pattern;

forming, over the substrate, a third insulating film with a relatively high dielectric constant and high mechanical strength;

planarizing the third insulating film by polishing so that the third insulating film thinly remains on the surface of the second insulating film;

forming an interconnect groove in the second insulating film and the first insulating film; and

forming a buried interconnect in the interconnect groove.

[Claim 7] The semiconductor device fabricating method of Claim 6, characterized in that:

the first insulating film includes an organic material as a principal constituent; and

the step of forming the interconnect groove in the second insulating film and the first insulating film comprises the step of performing etching using a mask pattern formed over the second insulating film to form the interconnect groove in the second insulating film, and then forming the interconnect groove in the first insulating film concurrently with the removal of the mask pattern.

[Claim 8] The semiconductor device fabricating method of Claim 6, characterized in that the mechanical strength of the second insulating film is between 4.0 GPa and 20.0 GPa.

[Claim 9] The semiconductor device fabricating method of Claim 6, characterized in that the dielectric constant of the second insulating film is between 3.5 and 4.5.

[Detailed Description of the Invention]

[Technical Field to which the Invention Belongs]

The present invention relates to a method for fabricating a semiconductor device, and more particularly, it relates to a method for forming a low dielectric film locally in a region of an insulating film where capacitance between interconnects is desired to be lowered.

[Prior Art]

Recently, in accordance with the increased degree of integration and the increased performance and operation speed of semiconductor integrated circuit devices, metal interconnects have been further refined and formed in structures of a larger number of levels. As one of means for attaining the refinement and the multi-level structures, a technique to use, as an interlayer insulating film, an insulating film with a low dielectric constant (hereinafter referred to as a low dielectric insulating film) has been proposed.

When a low dielectric insulating film is used for forming an interlayer insulating film, capacitance between interconnects can be lowered so as to avoid a problem of signal delay.

However, most of currently examined low dielectric insulating films have disadvantages of weakness against impact due to low mechanical strength and a poor heat dissipation due to low thermal conductivity.

In a technique proposed for overcoming these disadvantages, a low dielectric insulating film is used in a region of an interlayer insulating film where signal delay can lead to a serious problem, and an insulating film having a high dielectric constant but having high mechanical strength and high thermal conductivity, such as a silicon oxide film, is used in a region of the interlayer insulating film where signal delay does not lead to a serious problem.

Hereinafter, a method for locally forming a low dielectric insulating film between interconnects disclosed in Japanese Unexamined Patent Publication No. 11-135620 will be described with reference to FIGS. **8(a)** through **8(d)**.

First, as shown in FIG. **8(a)**, after forming metal interconnects **11** on a semiconductor substrate **10**, a resist pattern **12** is formed on a region of the semiconductor substrate **10** where capacitance between interconnects is particularly desired to be lowered.

Next, as shown in FIG. **8(b)**, a silicon oxide film **13** is formed by liquid growth on

a region of the semiconductor substrate **10** where the resist pattern **12** is not formed.

Then, as shown in FIG. **8(c)**, after removing the resist pattern **12**, a low dielectric insulating film **14** is formed over the entire surface of the semiconductor substrate **10**.

Subsequently, as shown in FIG. **8(d)**, a portion of the low dielectric insulating film **14** present over the silicon oxide film **13** is removed by CMP, thereby allowing the top face of the silicon oxide film **13** and that of the low dielectric insulating film **14** to be substantially flush with each other.

By repeatedly carrying out the aforementioned procedures, the low dielectric insulating film **14** can be selectively formed in regions where capacitance between interconnects is particularly desired to be lowered.

[Problems that the Invention is to solve]

When the interconnect pitch is reduced as a result of miniaturization of semiconductor integrated circuit devices, however, it becomes difficult to fill the low dielectric insulating film between interconnects, which causes a problem that the material for the low dielectric insulating film is restricted.

Also, since the low dielectric insulating film is generally poor in the mechanical strength, there arises a problem that defects such as peeling or scratch might be caused in the low dielectric insulating film in planarizing the low dielectric insulating film by the CMP.

In consideration of the aforementioned problems, an object of the invention is to definitely dispose a low dielectric insulating film between interconnects with a small interconnect pitch and to prevent the occurrence of defects, e.g., peeling or scratch, in the low dielectric insulating film.

[Means for Solving the Problems]

In order to achieve the object, a first method for fabricating a semiconductor device according to this invention includes the steps of: forming, on a substrate, a first insulating film with a relatively low dielectric constant and low mechanical strength; forming a mask pattern on a region of the first insulating film where capacitance between interconnects is desired to be lowered, and then patterning the first insulating film by performing selective etching using the mask pattern; forming, over the substrate, a second insulating film with a relatively high dielectric constant and high mechanical strength; planarizing the second insulating film by polishing so that the second insulating film thinly remains on the surface of the first insulating film; forming an interconnect groove in the first insulating film; and forming a buried interconnect in the interconnect groove.

In the first semiconductor device fabricating method according to this invention, the first insulating film with a low dielectric constant and low mechanical strength is patterned so that the first insulating film is present in the region where capacitance between interconnects is desired to be lowered, and thereafter the second insulating film with a high dielectric constant and high mechanical strength is formed. Therefore, the first insulating film with a low dielectric constant can be present in the region where capacitance between interconnects is desired to be lowered.

Also, since the surface of the first insulating film is not exposed in planarizing the second insulating film with high mechanical strength by polishing, defects such as peeling or scratch can be prevented from being caused in the first insulating film with low mechanical strength.

Furthermore, since the buried interconnect is formed by filling the metal film in the interconnect groove formed in the first insulating film with a low dielectric constant, the first insulating film can be definitely disposed between interconnects even when the interconnect pitch is small.

The first semiconductor device fabricating method preferably further includes the step of forming, over the first insulating film in which the buried interconnect is formed, a third insulating film for preventing diffusion of a metal included in the buried interconnect.

Thus, the metal included in the buried interconnect can be prevented from diffusing into the insulating film formed thereon.

In the first semiconductor device fabricating method, it is preferable that: the first insulating film and the second insulating film each include an inorganic material as a principal constituent; and the step of forming the interconnect groove in the first insulating film includes the step of forming an interconnect groove also in the second insulating film by selectively etching the first insulating film and the second insulating film at the same time.

Thus, the interconnect grooves can be simultaneously formed in the first insulating film and the second insulating film by one selective etching.

In the first semiconductor device fabricating method, the first insulating film includes an organic material as a principal constituent while the second insulating film includes an inorganic material as a principal constituent, and the method further includes, before or after the step of forming the interconnect groove in the first insulating film, the step of forming an interconnect groove in the second insulating film by selectively etching the second insulating film.

Thus, a material with a low dielectric constant can be used for forming the first insulating film. Also, even when the first insulating film and the second insulating film are made from different materials, the interconnect grooves can be formed in the first insulating film and the second insulating film.

A second method for fabricating a semiconductor device according to this invention includes the steps of: forming, on a substrate, a first insulating film with a

relatively low dielectric constant and low mechanical strength; forming, on the first insulating film, a second insulating film having mechanical strength higher than that of the first insulating film; forming a mask pattern on a region of the second insulating film where capacitance between interconnects is desired to be lowered, and then patterning the second insulating film and the first insulating film by selectively etching the second insulating film and the first insulating film using the mask pattern; forming, over the substrate, a third insulating film with a relatively high dielectric constant and high mechanical strength; planarizing the third insulating film by polishing so that the third insulating film thinly remains on the surface of the second insulating film; forming an interconnect groove in the second insulating film and the first insulating film; and forming a buried interconnect in the interconnect groove.

In the second semiconductor device fabricating method according to this invention, the first insulating film with a low dielectric constant and low mechanical strength is patterned so that the first insulating film is present in the region where capacitance between interconnects is desired to be lowered, and thereafter the third insulating film with a high dielectric constant and high mechanical strength is formed. Therefore, the first insulating film with a low dielectric constant can be present in the region where capacitance between interconnects is desired to be lowered.

Further, after the second insulating film with high mechanical strength has been formed on the first insulating film with low mechanical strength, the surface of the second insulating film is not exposed in planarizing the third insulating film by polishing, and therefore, defects such as peeling or scratch can be prevented from being caused in the first insulating film with low mechanical strength. Furthermore, since the buried interconnect is formed by filling the metal film in the interconnect groove formed in the first insulating film with a low dielectric constant, the first insulating film can be definitely disposed

between interconnects even when the interconnect pitch is small.

In particular, according to the second semiconductor device fabricating method, after the second insulating film with high mechanical strength has been formed on the first insulating film with low mechanical strength, the third insulating film is planarized by polishing, and the surface of the second insulating film is exposed so that the top face of the third insulating film and that of the second insulating film are substantially flush with each other. Therefore, it is possible to prevent a reduction in thickness of the insulating film present in the region where capacitance between interconnects is desired to be lowered.

In the second semiconductor device fabricating method, it is preferable that: the first insulating film includes an organic material as a principal constituent; and the step of forming the interconnect groove in the second insulating film and the first insulating film includes the step of performing etching using a mask pattern formed over the second insulating film to form the interconnect groove in the second insulating film, and then forming the interconnect groove in the first insulating film concurrently with the removal of the mask pattern.

Thus, the removal of the mask pattern and the formation of the interconnect groove in the first insulating film can be carried out concurrently, and therefore, the number of steps can be reduced.

In the second semiconductor device fabricating method, the mechanical strength of the second insulating film is preferably between 4.0 GPa and 20.0 GPa.

Thus, in planarizing the third insulating film by polishing, the occurrence of scratch in the second insulating film can be prevented.

In the second semiconductor device fabricating method, the dielectric constant of the second insulating film is preferably between 3.5 and 4.5.

Thus, even if the second insulating film is formed on the first insulating film with a low dielectric constant, an increase in capacitance between interconnects can be prevented.

[Embodiments of the Invention]

(First Embodiment)

Hereinafter, a method for fabricating a semiconductor device according to a first embodiment of the invention will be described with reference to the drawings.

First, as shown in FIG. **1(a)**, a first insulating film **101** with a thickness of 500 nm of a low dielectric film including an inorganic material as a principal constituent, such as a hydrogen silsesquioxane (HSQ) film, is formed by spin coating over a semiconductor substrate **100** on which lower interconnects not shown are formed. Thereafter, a first resist pattern **102** with a thickness of 2.0 μm is formed by known lithography on a region of the first insulating film **101** where capacitance between interconnects is particularly desired to be lowered.

Next, the first insulating film **101** is patterned through etching by using the first resist pattern **102** as a mask and the first resist pattern **102** is then removed as shown in FIG. **1(b)**. Thus, the first insulating film **101** remains merely in the region where capacitance between interconnects is particularly desired to be lowered.

Then, as shown in FIG. **1(c)**, a second insulating film **103** with a thickness of 700 nm of a plasma TEOS film (silicon oxide film) is formed by vapor growth over the silicon substrate **100**. Thereafter, as shown in FIG. **2(a)**, a portion of the second insulating film **103** present on the first insulating film **101** is removed by polishing in a CMP process, so that the second insulating film **103** with a thickness of about 10 nm to about 50 nm remains on the surface of the first insulating film **101**. The top face of a portion of the second insulating film **103** present on the first insulating film **101** becomes substantially flush with that of a portion of the second insulating film **103** under which the first insulating film **101** is

not present. In this case, since the first insulating film **101**, which is a low dielectric film, is not exposed, defects such as scratch are not caused.

Next, as shown in FIG. **2(b)**, a second resist pattern **104** having openings **104a** in interconnect groove forming regions is formed over the first insulating film **101** and the second insulating film **103**. Thereafter, the first insulating film **101** and the second insulating film **103** are etched by using an etching gas of, for example, a mixed gas of a CHF_3 gas and a CF_4 gas with the second resist pattern **104** used as a mask, thus simultaneously forming interconnect grooves **105** each having a depth of approximately 250 nm in the first insulating film **101** and the second insulating film **103** as shown in FIG. **2(c)**.

Subsequently, as shown in FIG. **3(a)**, a barrier metal layer of tantalum nitride and a seed layer of copper are successively deposited over the first insulating film **101** and the second insulating film **103** including the insides of the interconnect grooves **105**, and then, a copper film is grown on the seed layer by electro plating, thus depositing a metal film **106** composed of the barrier metal layer, the seed layer and the copper film so as to fill the interconnect grooves **105**.

Next, as shown in FIG. **3(b)**, a portion of the metal film **106** present over the first insulating film **101** and the second insulating film **103** is removed by a CMP process so as to form metal interconnects **107** serving as buried interconnects. Thereafter, as shown in FIG. **3(c)**, a third insulating film **108** of a silicon carbide film with a thickness of 50 nm for preventing diffusion of copper included in the metal interconnects **107** is formed by a plasma CVD process over the metal interconnects **107**, the firs insulating film **101** and the second insulating film **103**.

According to the first embodiment, since there is no need to fill a low dielectric film between metal interconnects with a small interconnect pitch, a low dielectric material

can be definitely disposed between the metal interconnects with a small interconnect pitch. Also, since the method does not include a step of filling a low dielectric material in a small space between the metal interconnects, the material for the low dielectric film can be selected from a wide range.

Further, after the first insulating film **101** has been formed, the CMP for allowing the top face of the first insulating film **101** to be substantially flush with that of the second insulating film **103** is performed on the second insulating film **103** of a silicon oxide film that is comparatively resistant to polishing; therefore, defects such as peeling and scratch are not caused in the first insulating film **101** that is a low dielectric film.

(Second Embodiment)

Hereinafter, a method for fabricating a semiconductor device according to a second embodiment of the invention will be described with reference to the drawings.

First, as shown in FIG. **4(a)**, a first insulating film **201** with a thickness of 500 nm of a low dielectric film including an organic material as a principal constituent, such as a polyallyl ether film, is formed by spin coating over a silicon substrate **200** on which lower interconnects not shown are formed. Thereafter, a second insulating film **202** of an insulating film having high mechanical strength, such as a silicon carbide film (mechanical strength: 8 GPa, dielectric constant: 4.5), is formed over the first insulating film **201** by a plasma CVD process. As the second insulating film **202**, a silicon carbide film is selected because it not only has mechanical strength but also has a dielectric constant lower than that of a silicon nitride film. Then, a first resist pattern **203** with a thickness of 2.0 μm is formed by known lithography on a region of the second insulating film **202** where capacitance between interconnects is particularly desired to be lowered.

Next, as shown in FIG. **4(b)**, the second insulating film **202** and the first insulating film **201** are etched by sequentially using a first etching gas of, for example, a mixed gas of

a CO gas and a CF_4 gas, and a second etching gas of, for example, a mixed gas of an H_2 gas and an N_2 gas with the first resist pattern **203** used as a mask, thereby patterning the second insulating film **202** and the first insulating film **201**, and thereafter, the first resist pattern **203** is removed. Thus, the second insulating film **202** and the first insulating film **201** remain merely in the region where capacitance between interconnects is particularly desired to be lowered.

Then, as shown in FIG. **4(c)**, a third insulating film **204** with a thickness of 700 nm of a plasma TEOS film (silicon oxide film) is formed over the silicon substrate **200** by vapor growth. Thereafter, as shown in FIG. **4(d)**, a portion of the third insulating film **204** present over the second insulating film **202** is removed by a CMP process so that the third insulating film **204** with a thickness of about 10 nm to about 50 nm remains on the second insulating film **202** and the surface of the third insulating film **204** is substantially flush. In this case, since the first insulating film, which is a low dielectric film, is not exposed, defects such as scratch are not caused.

Next, as shown in FIG. **5(a)**, a second resist pattern **205** having openings **205a** in interconnect groove forming regions is formed over the second insulating film **202** and the third insulating film **204**.

Then, the second insulating film **202** and the third insulating film **204** are etched by using an etching gas of, for example, a mixed gas of a CHF_3 gas and a CF_4 gas with the second resist pattern **205** used as a mask. Thus, as shown in FIG. **5(b)**, portions of the third insulating film **204** located on the second insulating film **202** are etched, and interconnect grooves **206** each having a depth of about 300 nm are formed in the third insulating film **204**; then, the supply of a CHF_3 gas is stopped, while the supply of a CO gas is started, thereby patterning the second insulating film **202**.

Subsequently, as shown in FIG. **5(c)**, etching is carried out by using an etching gas of, for example, a mixed gas of an H_2 gas and an N_2 gas to form the interconnect grooves **206** in the first insulating film **201**, and the second resist pattern **205** is removed.

Then, as shown in FIG. **6(a)**, a barrier metal layer of tantalum nitride and a seed layer of copper are successively deposited over the second insulating film **202** and the third insulating film **204** including the insides of the interconnect grooves **206**, and then a copper film is grown on the seed layer by electro plating, thus depositing a metal film **207** composed of the barrier metal layer, the seed layer and the copper film so as to fill the interconnect grooves **206**.

Next, as shown in FIG. **6(b)**, a portion of the metal film **207** present over the second insulating film **202** and the third insulating film **204** is removed by a CMP process so as to form metal interconnects **208**. Thereafter, as shown in FIG. **6(c)**, a fourth insulating film **209** of a silicon carbide film with a thickness of 50 nm for preventing diffusion of copper included in the metal interconnects **208** is formed by a plasma CVD process over the metal interconnects **208**, the second insulating film **202** and the third insulating film **204**.

According to the second embodiment, like the first embodiment, since there is no need to fill a low dielectric film between metal interconnects with a small interconnect pitch, the material for the low dielectric film can be selected from a wide range, and a low dielectric material can be definitely disposed between the metal interconnects with a small interconnect pitch.

Further, polishing in a CMP process for allowing the top face of the second insulating film **202** to be substantially flush with that of the third insulating film **204** is performed on the third insulating film **204** of a silicon oxide film, and therefore, defects

such as peeling and scratch are not caused in the first insulating film **201** that is a low dielectric film.

Furthermore, since the second insulating film **202** having high mechanical strength is formed on the first insulating film **201** having low mechanical strength, it is possible to prevent a reduction in thickness of the low dielectric films of the first insulating film **201** and the second insulating film **202** when the third insulating film **204** is polished by a CMP process.

It should be noted that as the first insulating film **201** in the second embodiment, an amorphous carbon film including an organic material as a principal constituent may be used instead of a polyallyl ether film. In that case, a mixed gas of an H_2 gas and an N_2 gas may be used as an etching gas.

In addition, as the first insulating film **201** in the second embodiment, a carbon-containing silicon oxide film may be used instead of polyallyl ether. In that case, a mixed gas of a CHF_3 gas and a CF_4 gas is preferably used as an etching gas.

Moreover, as the second insulating film **202** in the second embodiment, a silicon oxynitride film (mechanical strength: 10 GPa to 15 GPa, dielectric constant: 5.0 to 6.0) including an inorganic material as a principal constituent may be used instead of a silicon carbide film. The mechanical strength and dielectric constant of the silicon oxynitride film are each varied with a change in the mixture ratio of oxygen and nitrogen. In that case, a mixed gas of a CHF_3 gas and a CF_4 gas may be used as an etching gas.

Besides, as the second insulating film **202** in the second embodiment, a silicon nitride film (mechanical strength: 20 GPa, dielectric constant: 7.0) including an inorganic material as a principal constituent may be used instead of a silicon carbide film. In that case, a mixed gas of a CHF_3 gas and a CF_4 gas may be used as an etching gas.

FIG. 7 shows an example of the layout of a semiconductor integrated circuit device (system LSI chip), in which a CPU core block **A**, a logic circuit block **B1**, a logic circuit block **B2**, a DRAM array block **C1**, a DRAM array block **C2** and an SRAM array block **D** are provided on a silicon substrate. In the peripheral portion on the silicon substrate, a bonding pad region **E** is provided so as to surround these functional blocks. In such a semiconductor integrated circuit device, interconnects for mutually connecting the functional blocks (block-to-block interconnects) are formed.

In each of the aforementioned embodiments, the block-to-block interconnects for connecting functional blocks are formed in the region where the low dielectric film is formed. As a result, interconnect speed is secured in regions between the functional blocks where interconnect delay causes a problem.

In this manner, the block-to-block interconnects are formed in the region where the low dielectric film is formed in each of the embodiments, thereby lowering capacitance between interconnects and preventing interconnect delay.

Furthermore, in each of the embodiments, the bonding pad region is formed not from a low dielectric film but from a silicon oxide film with high mechanical strength because large stress is applied to this region in a bonding process.

[Effects of the Invention]

In the semiconductor device fabricating method according to the present invention, a first insulating film having a low dielectric constant can be present in a region where capacitance between interconnects is desired to be lowered.

Further, when a film such as a silicon oxide film, having mechanical strength higher than that of a low dielectric film, is polished, the low dielectric film is not exposed, and therefore, it is possible to prevent the occurrence of defects such as peeling or scratch in the low dielectric film having low mechanical strength.

Furthermore, since an insulating film having a low dielectric constant is not filled between interconnects, an insulating film having a low dielectric constant can be definitely disposed between the interconnects even if a space therebetween is small.

[Brief Description of the Drawings]

[FIG. **1**]

(**a**) through (**c**) are cross-sectional views for showing procedures in a method for fabricating a semiconductor device according to a first embodiment of the invention.

[FIG. **2**]

(**a**) through (**c**) are cross-sectional views for showing other procedures in the semiconductor device fabricating method according to the fist embodiment.

[FIG. **3**]

(**a**) through (**c**) are cross-sectional views for showing still other procedures in the semiconductor device fabricating method according to the first embodiment.

[FIG. **4**]

(**a**) through (**d**) are cross-sectional views for showing procedures in a method for fabricating a semiconductor device according to a second embodiment of the invention.

[FIG. **5**]

(**a**) through (**c**) are cross-sectional views for showing other procedures in the semiconductor device fabricating method according to the second embodiment.

[FIG. **6**]

(**a**) through (**c**) are cross-sectional views for showing still other procedures in the semiconductor device fabricating method according to the second embodiment.

[FIG. **7**]

A plane view for explaining a region where capacitance between interconnects is particularly desired to be lowered in a semiconductor integrated circuit device.

[FIG. **8**]

Cross-sectional views for showing procedures in a conventional method for fabricating a semiconductor device.

[Description of the Reference Characters]

100 silicon substrate

101 first insulating film

102 first resist pattern

103 second insulating film

104 second resist pattern

104a opening

105 interconnect groove

106 metal film

107 metal interconnect

108 third insulating film

200 silicon substrate

201 first insulating film

202 second insulating film

203 first resist pattern

204 third insulating film

205 second resist pattern

205a opening

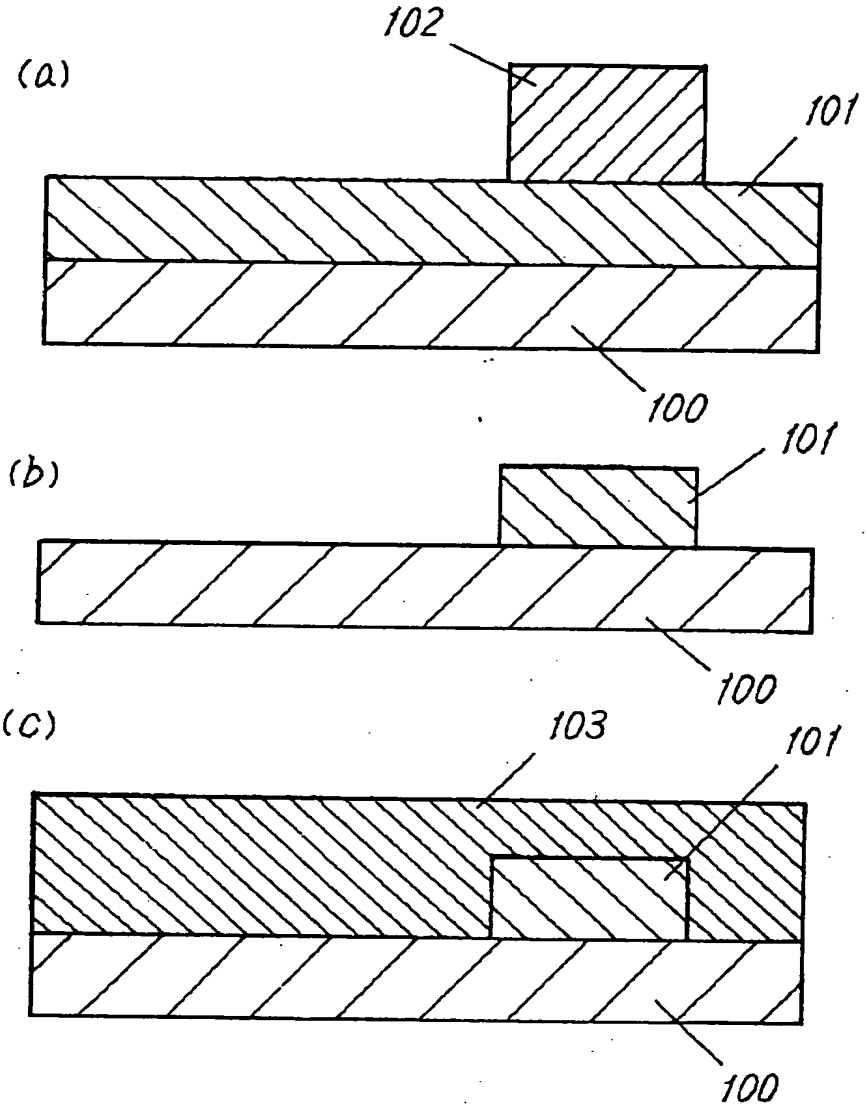
206 interconnect groove

207 metal film

208 metal interconnect

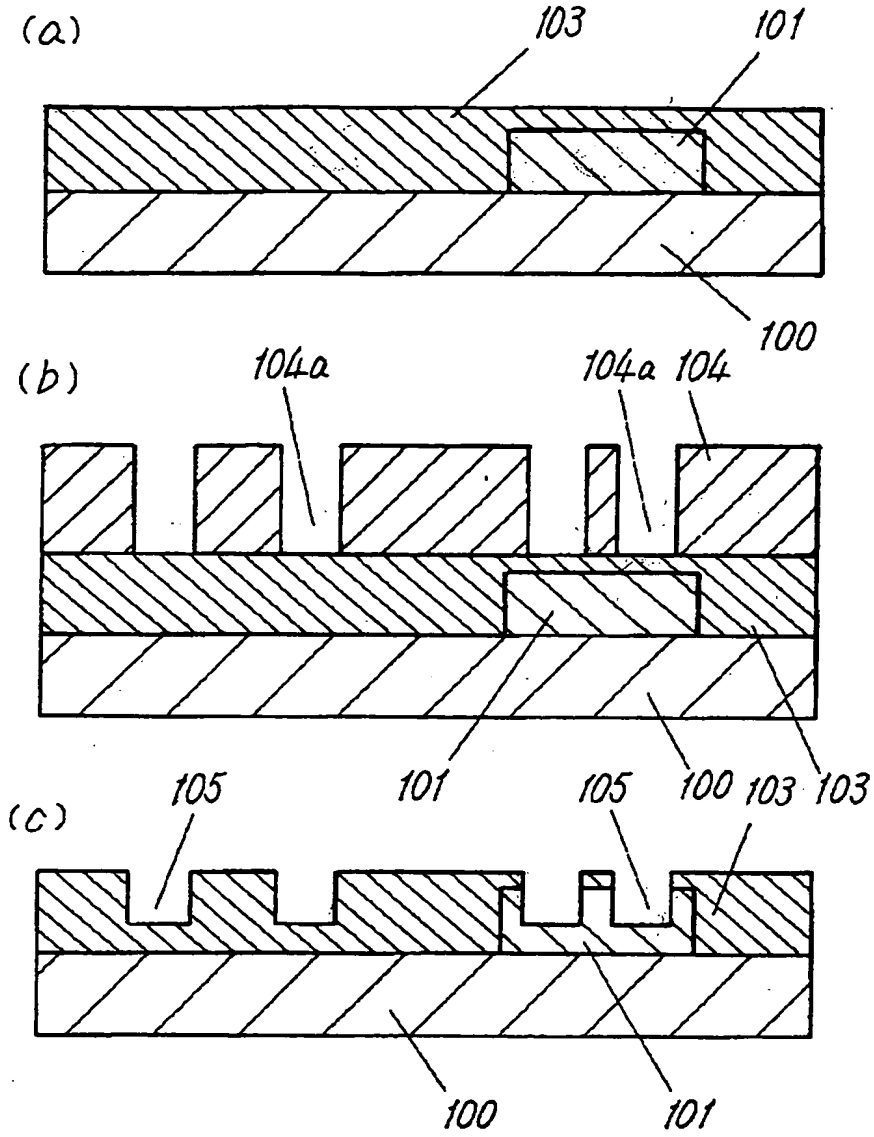
209 fourth insulating film

【書類名】　図面 → Drawings
↳ Name of the Document
【図１】
↓
FIG. 1



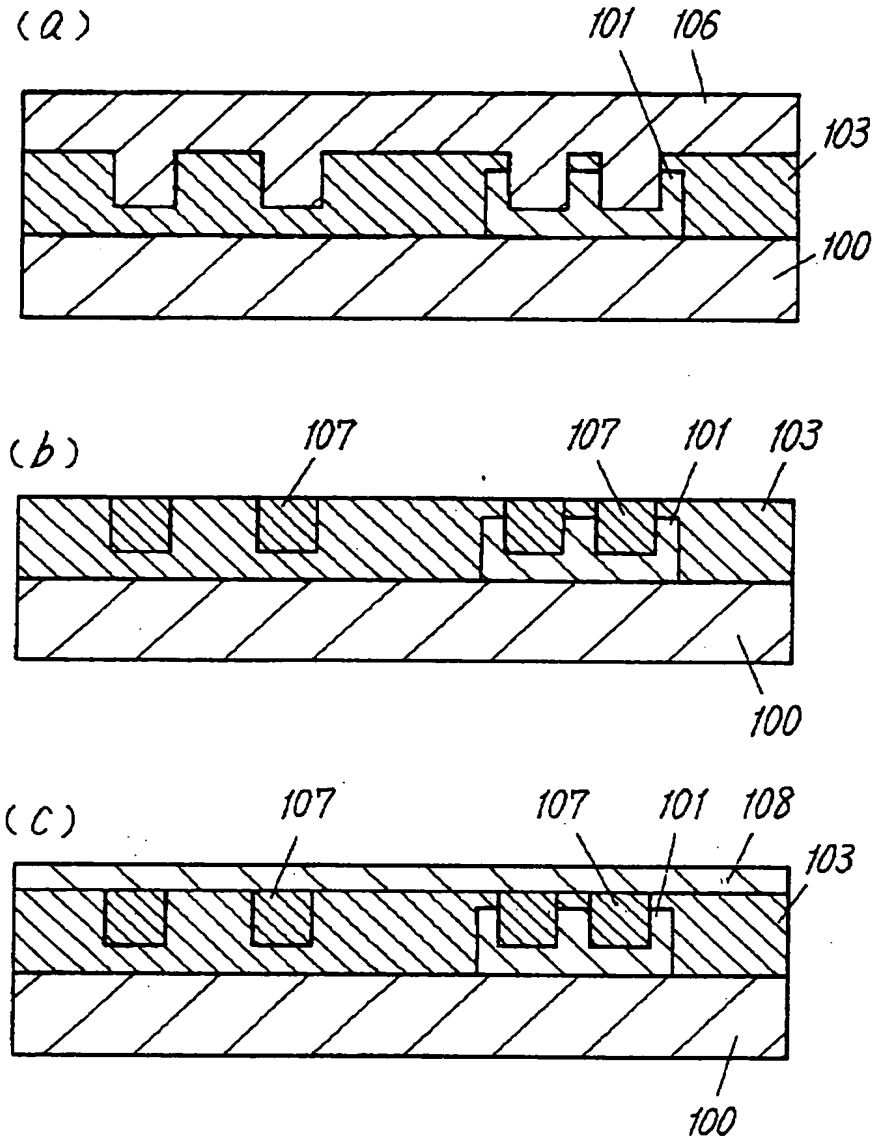
【図２】

FIG. 2



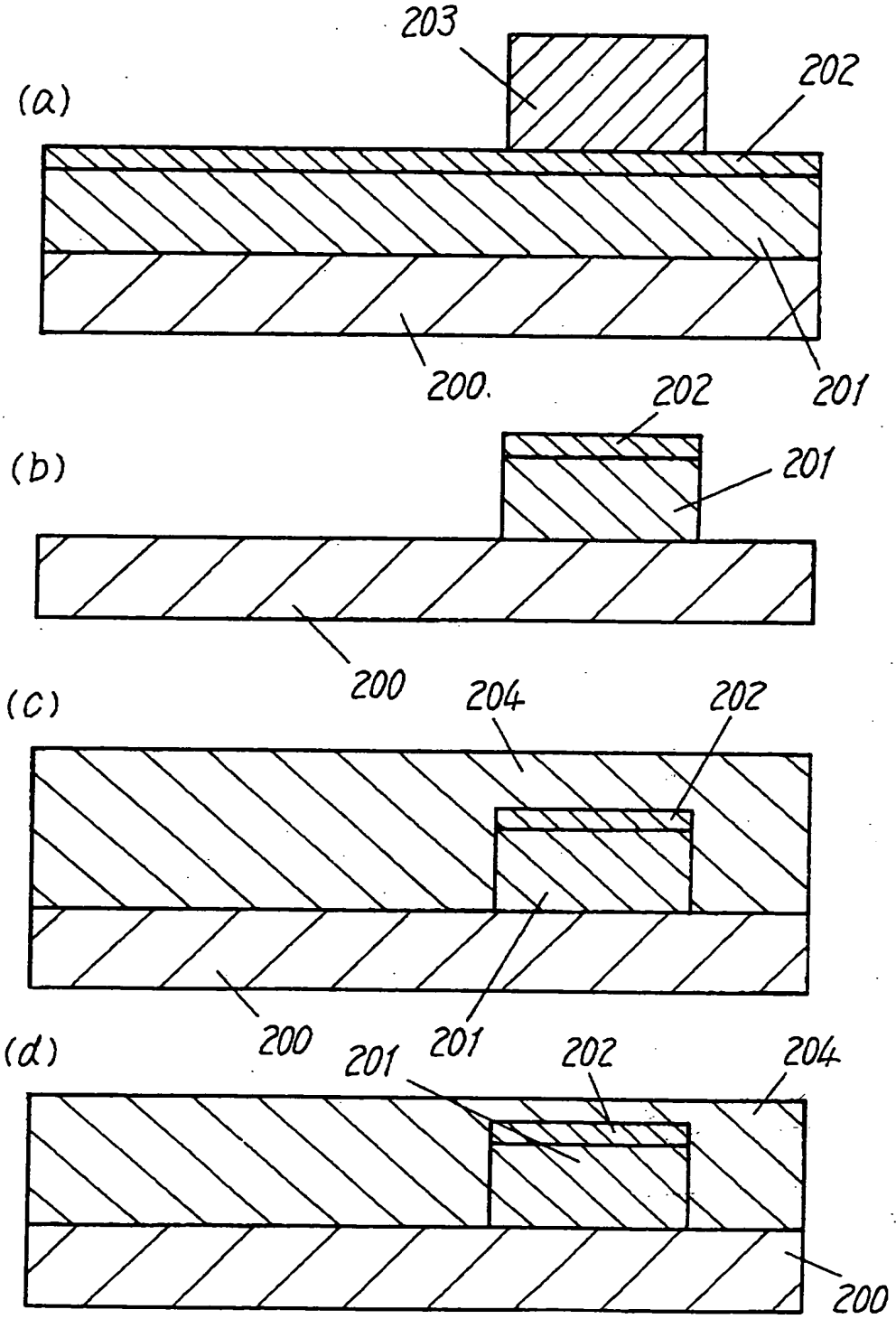
【図３】

FIG. 3



【図４】

FIG. 4


(a)
203
202
200
201
(b)
202
201
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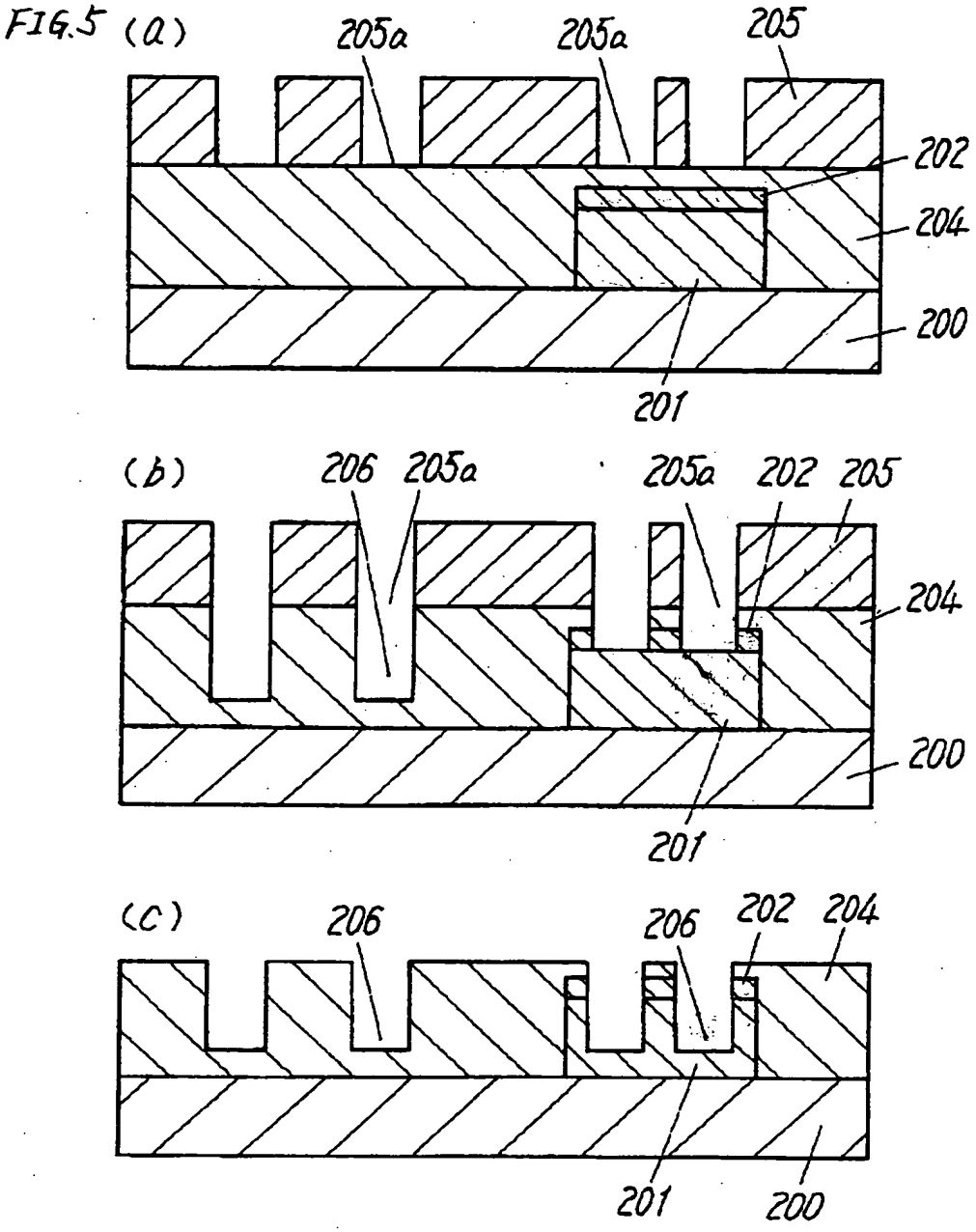
(c)
204
202
200
201
(d)
201
201
202
204
200

【図５】

FIG.5


(a)
205a
205a
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202
204
200
201
(b)
206
205a
205a
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205
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(c)
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206
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204
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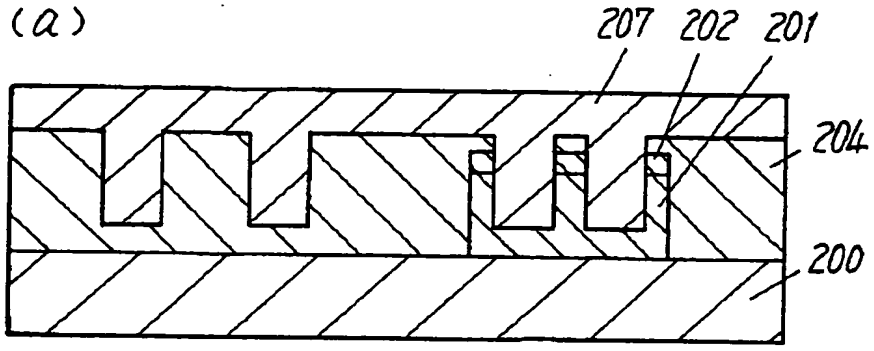
200

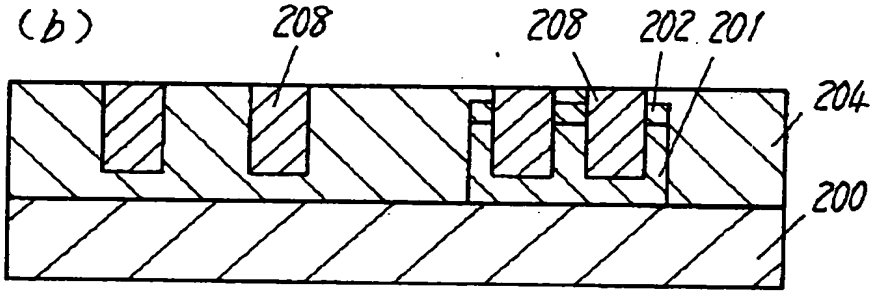
【図６】

FIG.6

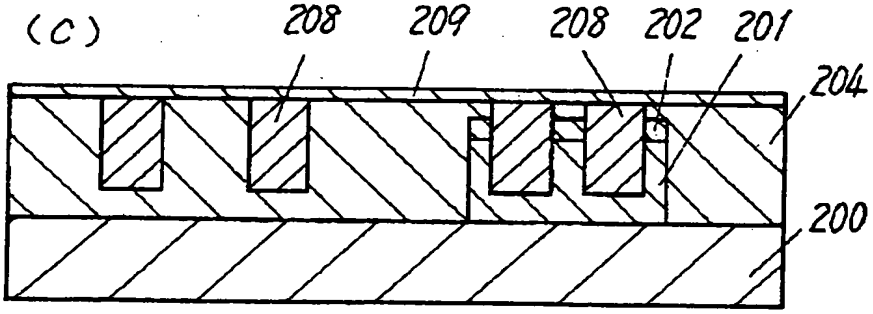
(a)


207
202
201
204
200

(b)


208
208
202
201
204
200

(c)


208
209
208
202
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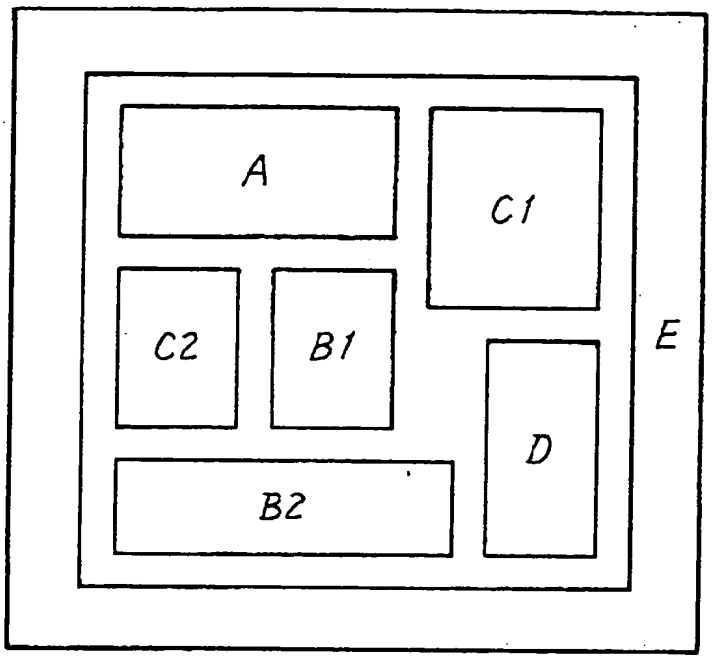
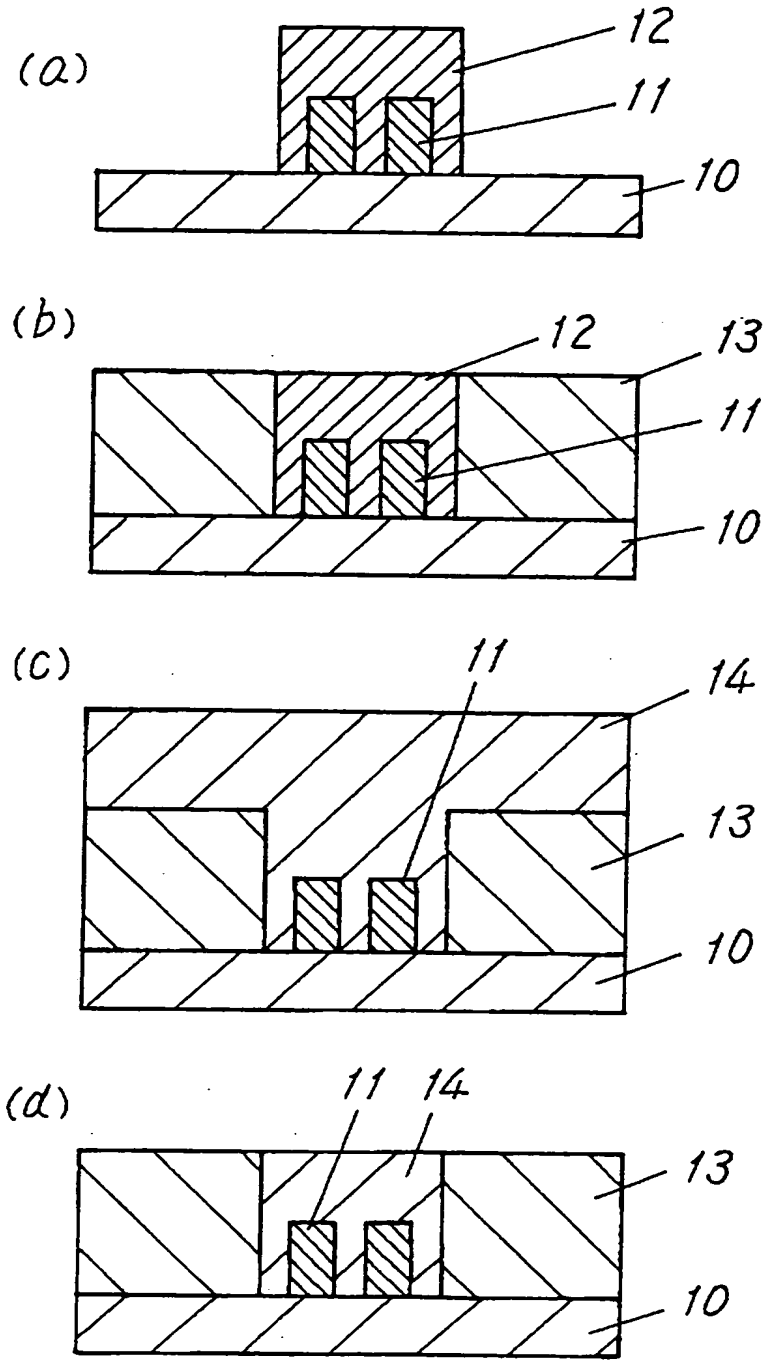
【図７】

FIG.7



【図８】

FIG.8



[Name of the Document] Abstract

[Abstract]

[Problem] To definitely dispose a low dielectric insulating film between interconnects with a small interconnect pitch and to prevent the occurrence of defects, e.g., peeling or scratch, in the low dielectric insulating film.

[Solution] A first insulating film **101** of an inorganic low dielectric film is formed on a silicon substrate **100**, and then the first insulating film **101** is patterned so that the first insulating film **101** remains in a region where capacitance between interconnects is particularly desired to be lowered. A second insulating film **103** of a silicon oxide film is formed over the silicon substrate **100**, and thereafter the second insulating film **103** is planarized by polishing in a CMP process so that the second insulating film **103** thinly remains on the surface of the first insulating film **101**. After interconnect grooves **105** have been formed in the first insulating film **101** and the second insulating film **103**, the interconnect grooves **105** are filled with a metal film to form metal interconnects.

[Selected Figure] FIG. **2**